# Chapter 1. SPI Debug Interface

## 1.1 Overview

SPI debug interface is developed to access whole system registers from PC side when CPU/DSP is not ready. It can be easily and simply used to tune DDR/PLL setting bypassing CPU/DSP. This IP has one external SPI interface and provide APB bridge to connect NOC system. The APB clock is 250MHz, and SPI interface clock can be up to 35MHz.

## 1.2 Block Diagram



Figure 1.1 SPI debug interface diagram

## 1.3 Features

* The Sirius SPI debug interface offers the following features：  
  ■ SPI command format with big endian  
  ■ APB access with little endian  
  ■ Access whole system registers